Innovations in Glass-Based Solutions for Advanced Semicon Packaging & Consumer Electronics

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Presentation Outline

- Why glass in semicon packaging & CE?
- Enabling glass adoption
- Innovations in glass-based solutions:
  - Advanced Packaging Carriers
  - Wafer-Level Optics
  - Augmented Reality

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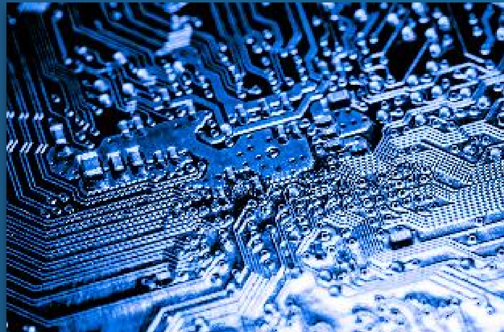
Key megatrends are driving the need for glass in semiconductor processes

Trends

Applications

1. More functional, compact chips



Advanced packaging

2. Highly accurate, miniaturized sensors

Wafer-level optics

3. Faster, seamless connections

Low-loss & high linearity RF components

4. Engaging, immersive interfaces

Waveguide displays for augmented reality

Glass-based solutions enable all of these applications

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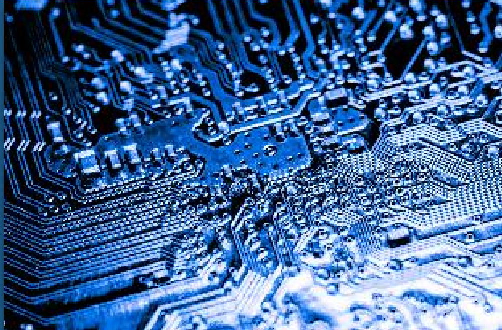
Glass is an ideal enabling material for these applications

Applications

	1. Advanced Packaging	*2. Wafer-Level Optics*	*3. Low-loss, high linearity RF*	*4. Waveguide-based augmented reality*
				
Why Glass?	✓ Multiple CTEs & high stiffness ✓ Transparent ✓ Scalable	✓ High purity ✓ Multiple CTEs, refractive indices, & thicknesses ✓ Ultra-low TTV and warp	✓ Low dielectric loss across wide frequency spectrum ✓ CTE match to Si possible	✓ Multiple refractive indices ✓ Precision surface

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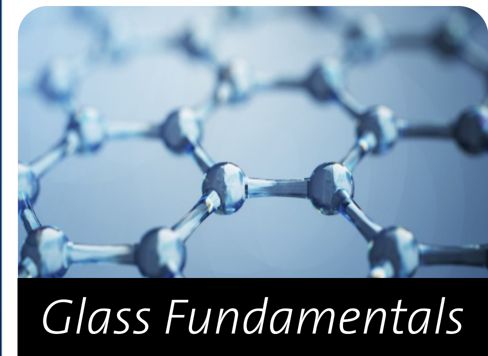
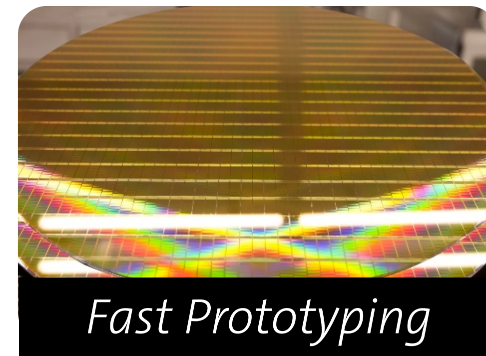
Customer Requirement #1

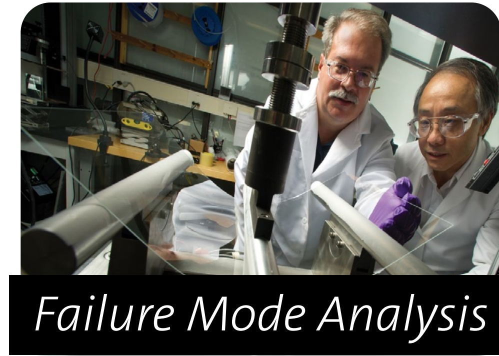
Deep technical engagement that's tailored to every development stage

Customer's Product Development Stages

Supporting Services & Insight







Delivers shorter learning cycles, higher yields, improved product reliability

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Customer Requirement #2

Customized material science expertise applied to specific applications

Application Examples:	Fan-Out Wafer-Level Packaging	Wafer-Level Optics & Silicon on Glass	Waveguide Eyepieces for Augmented Reality
Customer Requirements:	***Minimize in-process warp***	***Use glass in front-end processes***	***Maximize field of view and visual experience***
Solutions:	***Advanced Packaging Carriers with high Young's Modulus and fine granularity CTEs***	***HPFS®, an industry-leading fused silica that's 100% Si02***	***High refractive index glass wafers with ultra-low TTV***

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Advanced packaging needed to deliver pace of performance improvement

- The number of foundries investing in subsequent nodes is reducing
- Time between nodes is increasing
- Many believe that advanced packaging is needed to deliver pace of performance improvements
    - *Example: Fan-out Packaging (FO)*

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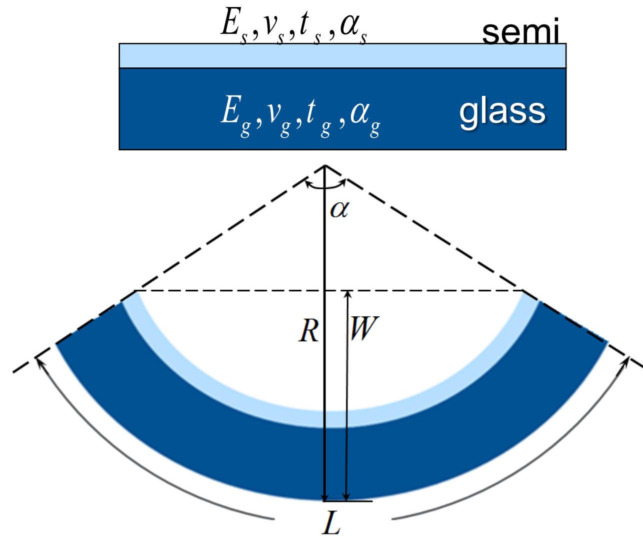
CTE mismatch causes in-process warp



Under typical fan-out conditions, in-process warp follows a simplified formula showing its dependence on:

1. CTE mismatch between glass & the composite semi material
2. Inverse of glass Young's modulus
3. Inverse of square of glass thickness

$$\approx 0.75L^2 \Delta\alpha \Delta T \frac{E_s(1-v_g)}{E_g(1-v_s)} \frac{t_s}{t_g^2}$$

E : Young's modulus; v : Poisson's ratio; t: Glass thickness;
α : Coefficient of thermal expansion; T : Temperature.
g: glass; s: semiconductor layers (MC + redistribution layers + die)

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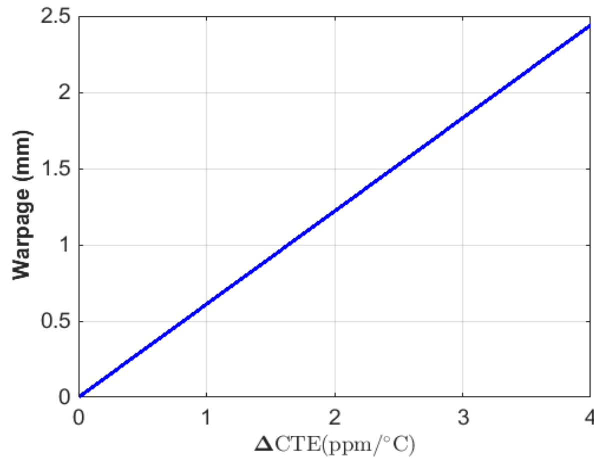
Three glass-based levers to minimize in-process warp

1. Decrease Δ CTE



$E_g = 70GPa$; $E_s = 20GPa$;

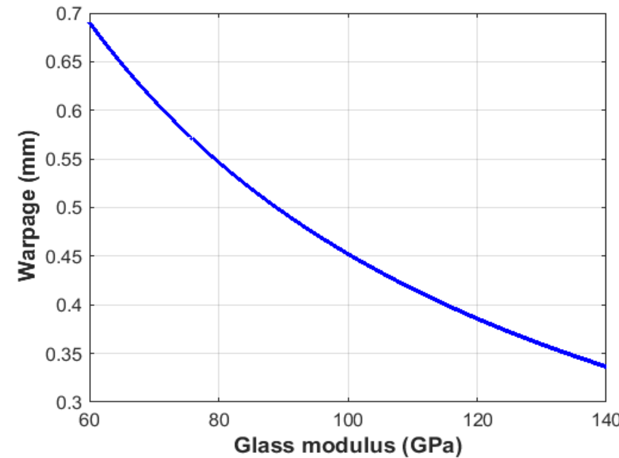
$v_g = 0.22$; $v_s = 0.35$;

$t_g = 1.1mm$; $t_s = 0.15mm$;

$T_{room} = 20°C$; $T_{process} = 250°C$;

Challenge: Package CTE changes throughout processing

2. Increase modulus



$E_s = 20GPa$;

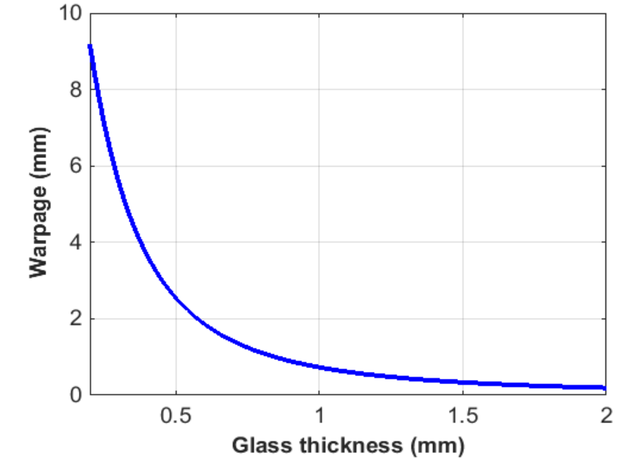
$v_g = 0.22$; $v_s = 0.35$;

$t_g = 1.1mm$; $t_s = 0.15mm$;

$\Delta CTE = 1.0ppm/°C$;

$T_{room} = 20°C$; $T_{process} = 250°C$;

3. Increase thickness



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$t_s = 0.15mm$;

$\Delta CTE = 1.0ppm/°C$;

$T_{room} = 20°C$; $T_{process} = 250°C$;

Challenge: Diminishing returns beyond 1 mm

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Advanced Packaging Carriers

Corning Advanced Packaging Carriers?

1. Fine granularity of CTE's-minimize Δ CTE
2. High Stiffness: Increased YM & optimized thickness
3. 4-6 week lead time for samples

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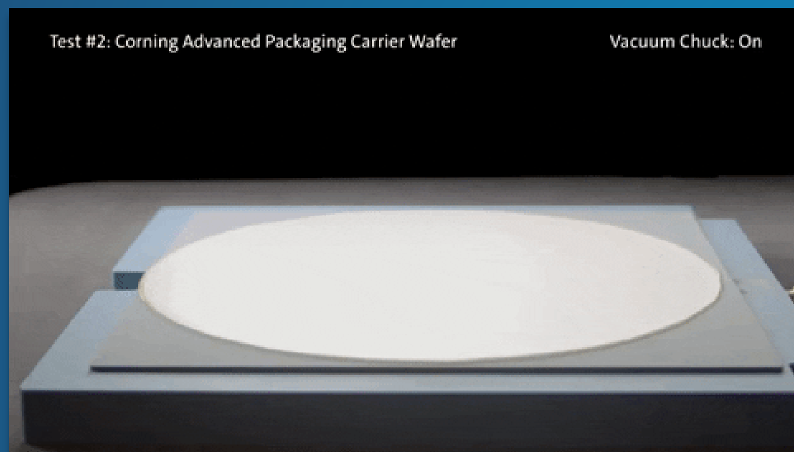
Market reaction to Corning Advanced Packaging Carriers (APC)

Currently being used in **20** customer projects



Customer: APC reduced in-process warp by **150 µm**

Awarded 3D Incites 2019 **Material Supplier of the Year** for APC

Featured in July/Aug. issue of **Chip Scale Review**

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Innovative Glass-Based Solution: *Wafer-Level Optics*

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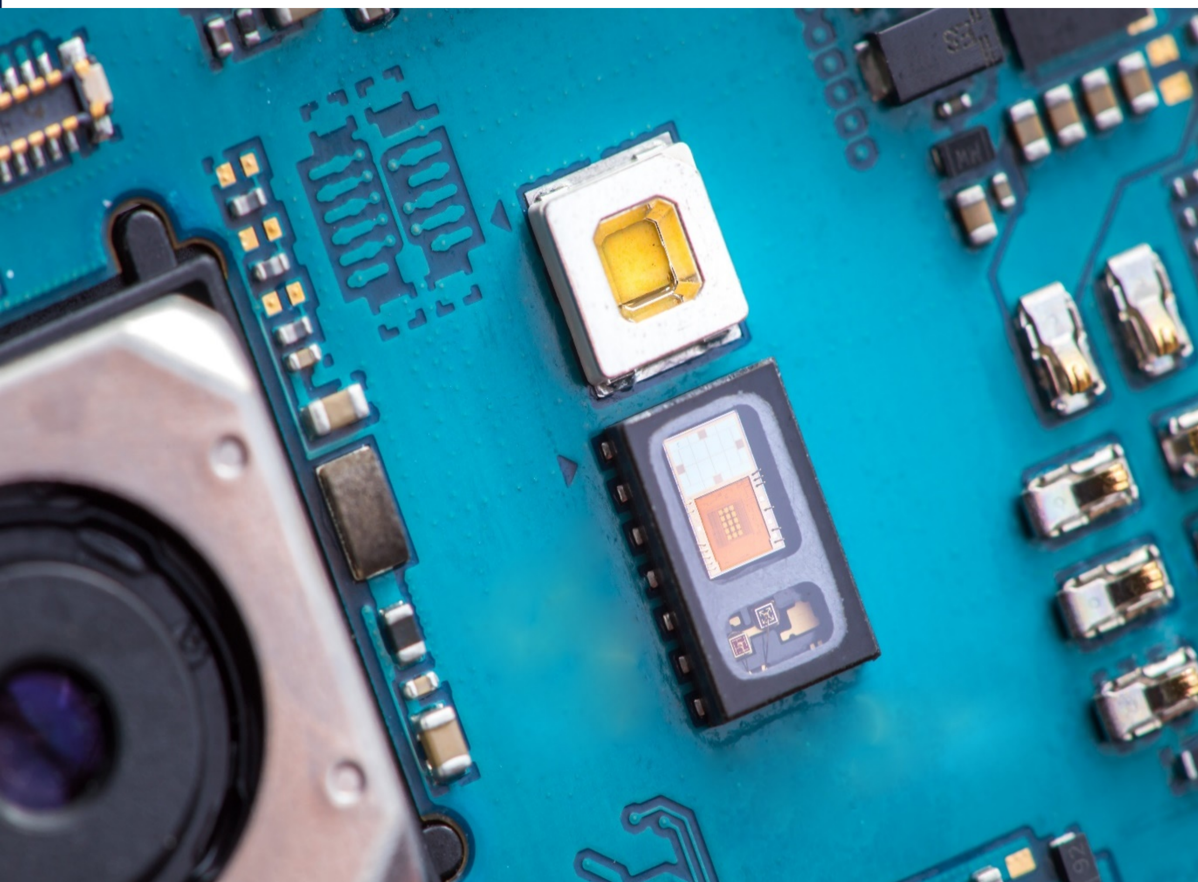
Optical sensors need to get smaller and more accurate. Enter, wafer-based ***semicon processes…***



Miniaturization is driving **changes in manufacturing** of these sensors

Front-end processes (FEOL)

Back-end processes (BEOL)

Each with a set of **challenges**

Front-end processes (FEOL):
- Contamination
- TTV
- Warp

Back-end processes (BEOL):
- Package stacking tolerance
- Delamination

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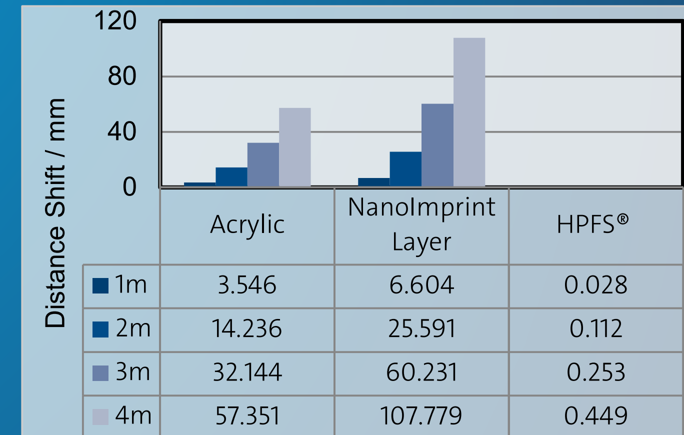
Fused silica is FEOL-compatible

Corning HPFS® Fused Silica:

- ✓ Ultra-pure material: 100% SiO_2
- ✓ Extreme thermal durability: Near-zero CTE
- ✓ Track record of success: HPFS has enabled 300M+ devices to date

Why HPFS is ideal for 3D sensing

High thermal durability!



	Acrylic	NanoImprint Layer	HPFS®
1m	3.546	6.604	0.028
2m	14.236	25.591	0.112
3m	32.144	60.231	0.253
4m	57.351	107.779	0.449

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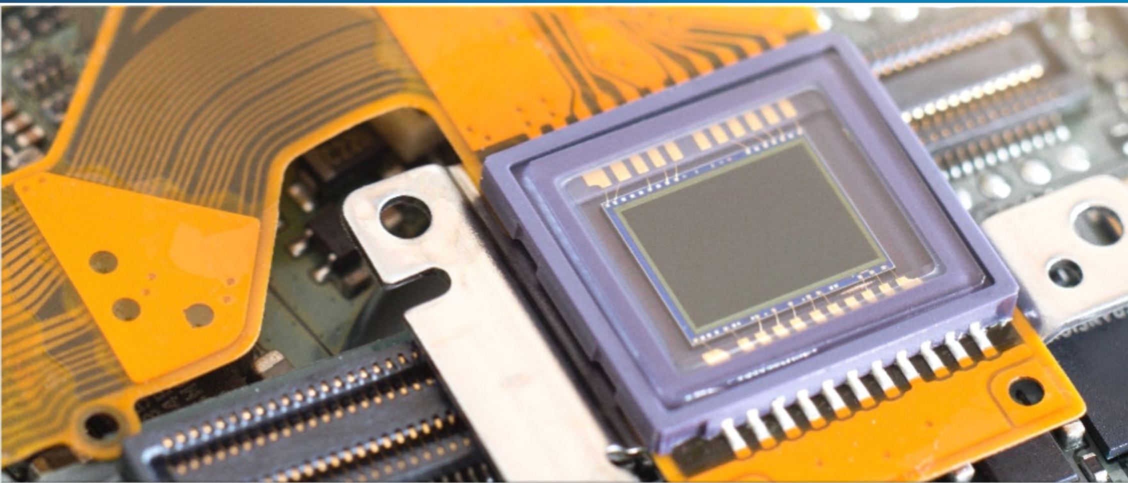
BEOL applications require a wide range of optical glasses

Top Challenges

1 Package stacking tolerance

2 Delamination



How Glass Addresses

- ✓ Tight glass geometric tolerances deliver lower stacking variance
  Corning optical glasses have:
  - ✓ *1.8x lower avg. thickness variation*
  - ✓ *1.5x lower average TTV*
  - ✓ *2.7x lower warp*
- ✓ Customizing glass CTE can lower delamination stress by up to 50%, driving enhanced device reliability
  - ✓ *Corning provides modeling to pick optimal CTE from its portfolio*

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Innovative Glass-Based Solution:
High-index glass and tools for Augmented Reality

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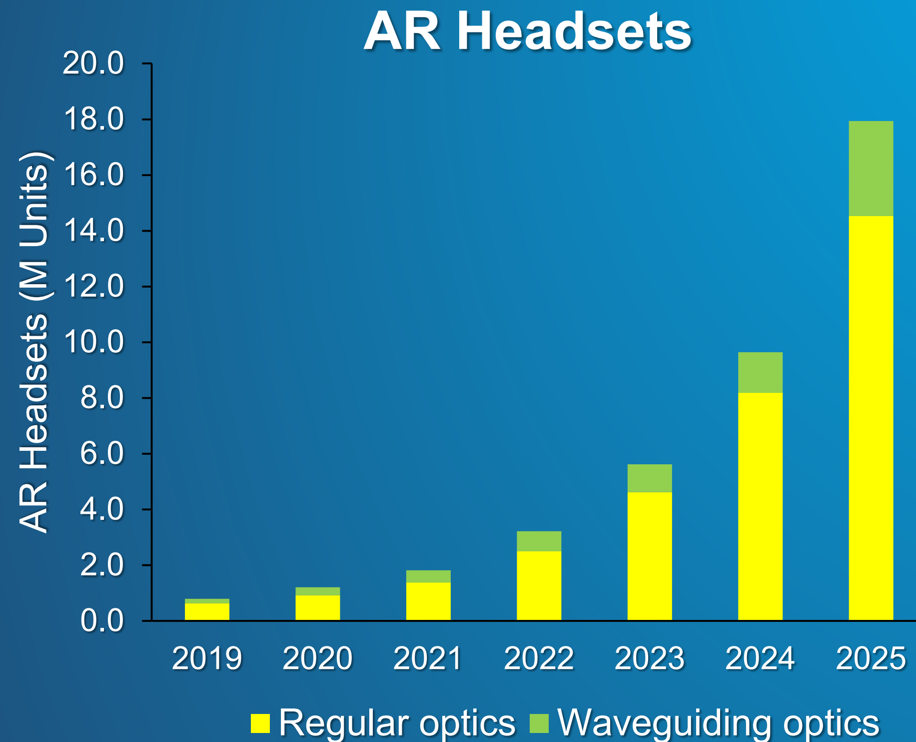
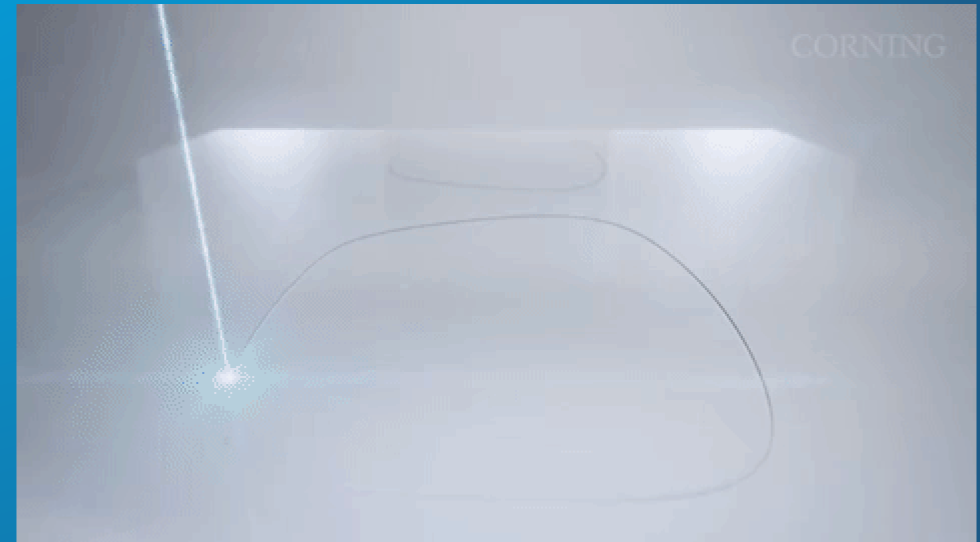
AR headset demand is coming; ***Glass with semicon-like processing*** will enable engaging experiences with these devices



Source: Yole Developpement

Waveguides require ultra-flat, high refractive index glass with gratings for a wide field of view



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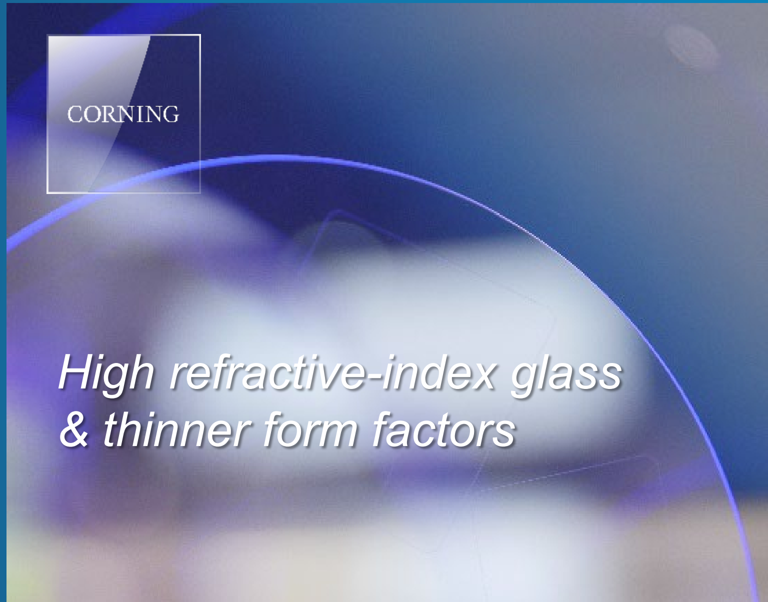
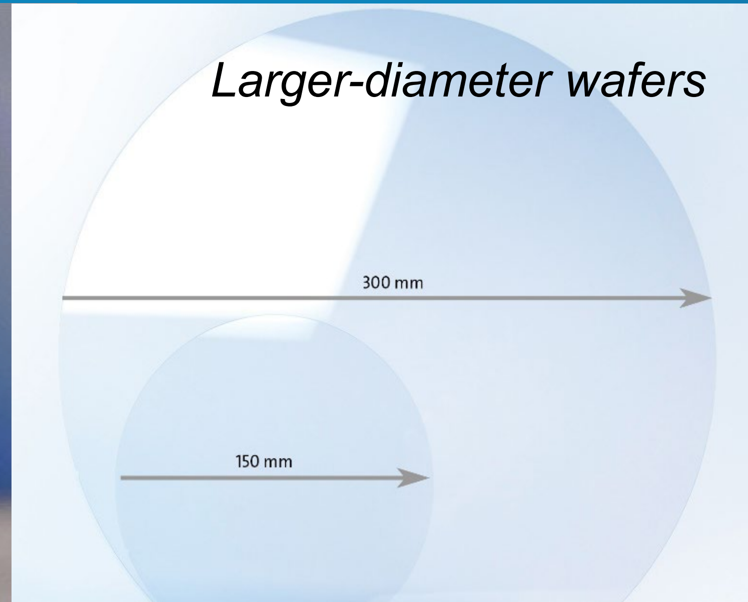
Corning is enabling the emerging AR/MR supply chain

Reduced BoM cost

Customer Challenges	Wider field of view & lighter device	Higher equipment & material utilization	Higher throughput
Corning Solutions	*High refractive-index glass & thinner form factors*	*Larger-diameter wafers*	*Automated laser glass-cutting machines*





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