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SPECIAL SECTION PAPER

WILEY

# Wrap-around electrodes for microLED tiled displays

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**Abstract**

The authors have developed a process to create wrap-around electrodes (WAEs) on glass for use in tiled microLED display applications. The electrodes have small size and spacing, low resistance, and good reliability. In addition, an opaque overcoat protects the edges of the tiles and reduces seam visibility. These electrodes allow bezel-free tiled operation for high-resolution displays.

**KEYWORDS**

bezel-free, MicroLED, seamless display, tiled display, wrap-around electrode

## 1 | OBJECTIVE AND BACKGROUND

MicroLEDs have great potential for future displays. High dynamic range, brightness, and low power consumption are a few of the potential benefits. Because the technology is still relatively new, current best practices are to make microLED tiles and then assemble the tiles into large displays.[1] To achieve high-resolution displays with small pixel pitches, bezel-free operation is required. While through glass vias (TGVs) can be used to connect the microLEDs to the drive electronics,[2] wrap-around electrodes are another method to complete the electrical connection. Although Corning has developed TGV panel making technology, the focus of this paper is on technology developed to provide bezel-free wrap-around electrodes on Corning Lotus™ NXT glass tiles. Corning Lotus™ NXT glass has excellent dimensional stability, thermal stability, and surface quality to enable MicroLED displays. The low total pitch variation and thickness variations along with the stable dimensions at high temperature oxide/LTPS TFT processes enables high resolution TFTs.

The objective is to create tiles with wrap-around electrodes as shown in Figure 1, which is an illustration that consists of two tiles that are in close proximity so that there is no change in pixel pitch from one tile to another. Key features of these tiles are that the edges have small, slightly curved chamfers, and a thin metallic electrode provides connection from the front surface to back surface. The chamfered edges increase the edge strength of the tiles and improves the continuity of the metal electrodes. In addition, the electrodes are covered with an opaque overcoating that provides both protection of the electrodes from mechanical/contact damage and electrical insulation between adjacent tiles. The opaque overcoat also reduces reflections from the tile edges and make the seams less visible. The tiles also have very tight dimensional tolerances for length, width, squareness, and uniformity of the curved chamfer required for tiling of larger displays.

We have developed a process to create glass tiles with wrap-around electrodes from large sheets of glass as shown in Figure 2. First, large panels of patterned glass are singulated into tiles with high precision and dimensional accuracy. The tiles are edge finished to provide a slightly curved chamfer and remove any chips from the singulation step. Subsequently, metallic electrodes are deposited around the edge of the tiles. Finally, an opaque edge coating is applied to the edges to protect the electrodes and provide electrical insulation between adjacent tiles.

  

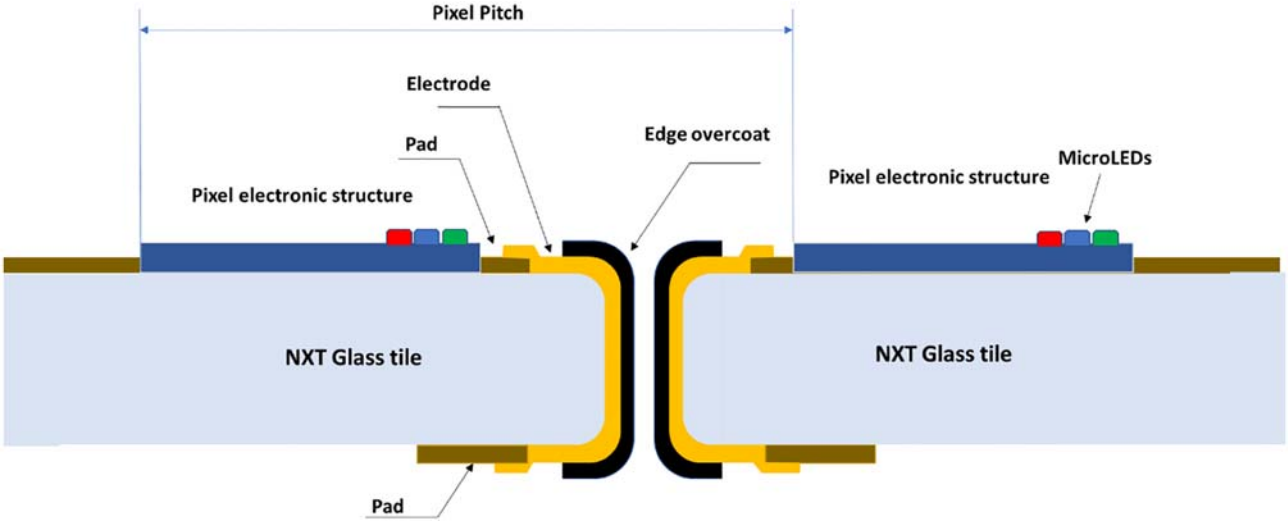


**FIGURE 1** Cross sectional schematic of a MicroLED tile with a wrap-around electrode

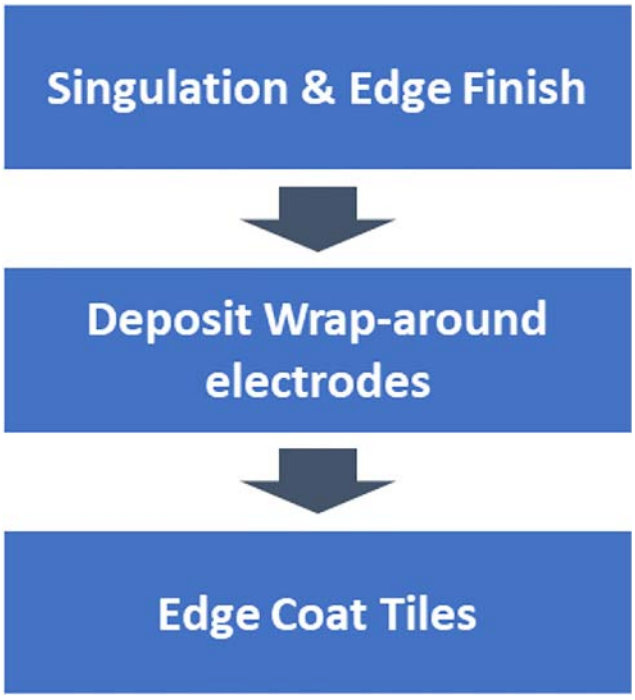


**FIGURE 2** Process used to fabricate tiles with wrap-around electrodes

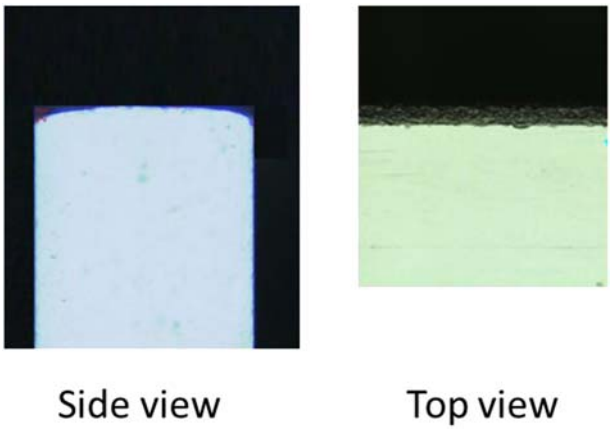


**FIGURE 3** Typical edge finishing profiles for singulation and edge finishing

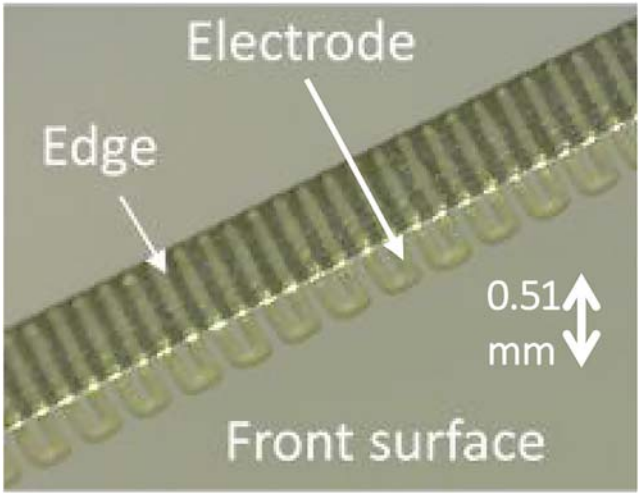


**FIGURE 4** Fifty micron wrap-around electrodes with 50 micron spacing on 0.5-mm-thick NXT glass

**TABLE 1** Singulation and edge finishing capability

| Key parameter | |
|---|---|
| Side straightness | ±0.6 μm |
| Side perpendicularity | $90^{o} \pm 0.006^{o}$ |
| Dimension tolerance | ±3 μm |
| Chamfer width | 37 μm ± 9 μm |

## 2 | RESULTS

### 2.1 | Singulation and edge finishing

We have developed equipment and processes to singulate and edge finish large sheets of patterned glass. Typical panel sizes are around 300 × 400 mm, and tile sizes range from 100 to 300 mm. The edge accuracy and precision in singulation are on the order of 10 microns, and the chamfer tolerances are typically <60 microns. Control of the chip size is also critical to enable continuity of the electrodes that wrap around the edge of the glass. The current 1 sigma capability is summarized in Table 1, with typical edge profiles shown in Figure 3.

### 2.2 | Electrode deposition

The electrode deposition process creates electrodes that can range from 100 microns wide with 100 micron spacing down to 20 microns wide with 20 micron spacing. The thickness of the deposited electrodes can range from 1 to 10 microns. The deposited electrodes consist of typical metals; silver, copper or gold, custom developed inks. Sheet resistance of 0.02 Ω/□ can be achieved. Figure 4 shows a typical wrap around electrode. In addition, the contact resistance between the electrodes and metallic contact pads has been characterized. The line pad structure is shown in Figure 5. Results have been obtained using 4-point probe Kelvin resistance measurement method. Contact resistance for gold is 0.06 Ω.

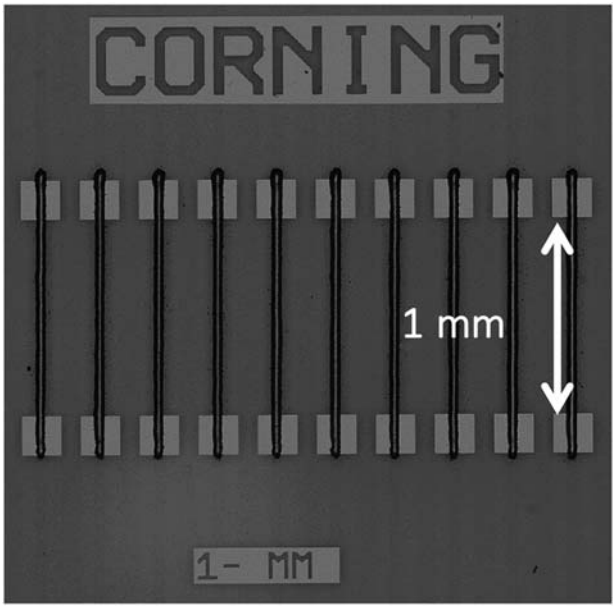


**FIGURE 5** Metal lines printed on gold pads. Kelvin probe measurements on pads and lines yield contact resistance

Various reliability tests of the electrodes have also been performed. As can be seen from Figure 6, cross hatch adhesion testing of a 5 micron thick layer of the electrode material to glass resulted in a value of 5B[3]. In addition, a modified cross hatch test was performed on the electrodes. Lines that are nominally 50 microns wide, with 100 micron spacing, were deposited on the glass surface and then the crosshatch was performed perpendicular to the lines. The same tape used in the ASTM standard was then applied and removed. The resulting image of the test is shown in Figure 7, demonstrating excellent adhesion. Additionally, the electrodes have been exposed to accelerated lifetime testing of 1000 h at

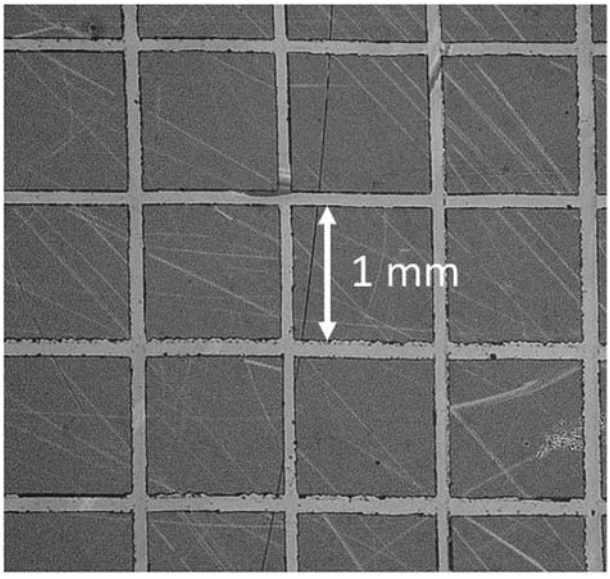


**FIGURE 6** 5B adhesion from crosshatch test for 5-micron-thick layer of electrode ink

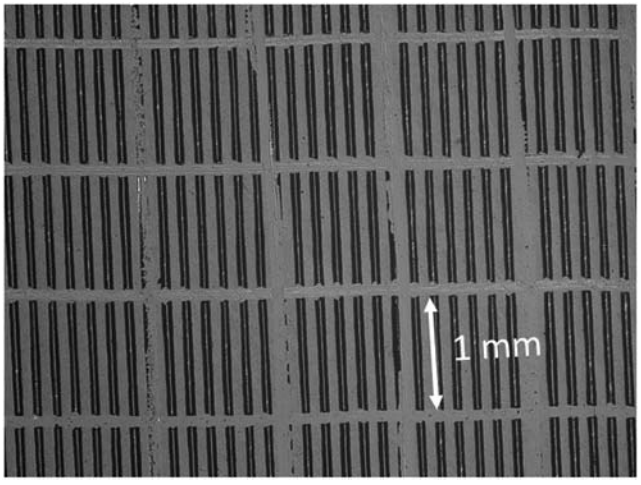


**FIGURE 7** "5B" like adhesion for modified cross hatch test on 50-micron-wide electrodes

85°C/85% relative humidity with no degradation in electrical performance. Finally, the electrodes have been subjected to high current at elevated temperatures (300 mA at 85°C) with no permanent change in electrical properties. Table 2 summarizes the electrical performance.

## 2.3 | Edge coating

The final process step is to provide an opaque edge coating to protect the electrodes from impact damage and provide electrical insulation between adjacent tiles. In addition, making the edge black helps hide the seam of the tile by managing light reflections. Typical example of the edge coating is shown in Figure 8, and the performance of the edge coating is summarized in Table 3. The coating has 5B adhesion as shown by cross hatch measurement in Figure 9.

## 2.4 | TFT performance

Functioning LTPS TFTs driven by wrap-around electrodes have also been fabricated. Samples were made with TFTs positioned 125 microns from a finished edge. Wrap-around

**TABLE 2** Summary of electrode performance

| Key parameter | |
|---|---|
| Sheet resistance | 0.02 Ω/□ |
| Contact resistance with gold | 0.06 Ω |
| Change in resistance after 1000 h of 85C/85%RH | 0.2 ± 1% |
| Change in resistance after 300-mA cycle | 0% |

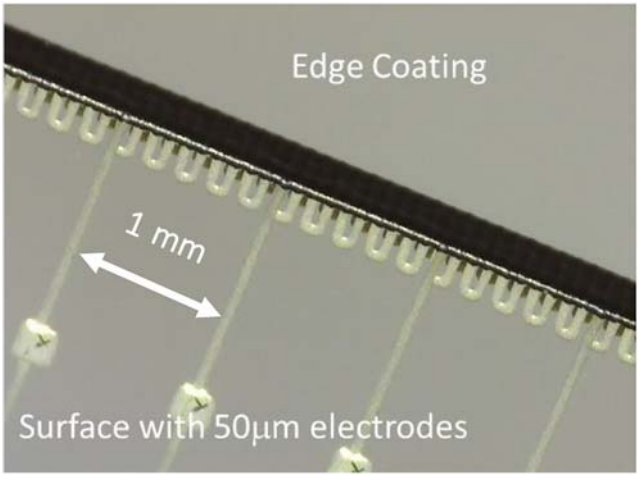


**FIGURE 8** Edge-coated 50 micron wrap-around electrode with measurement pads

**TABLE 3** Edge coating performance

| Key parameter | |
|---|---|
| Coating thickness (µm) | 4 |
| Surface overlap (µm) | 60 ± 25 |
| Optical density | 2.3 ± 0.1 |
| Crosshatch adhesion | 5B |

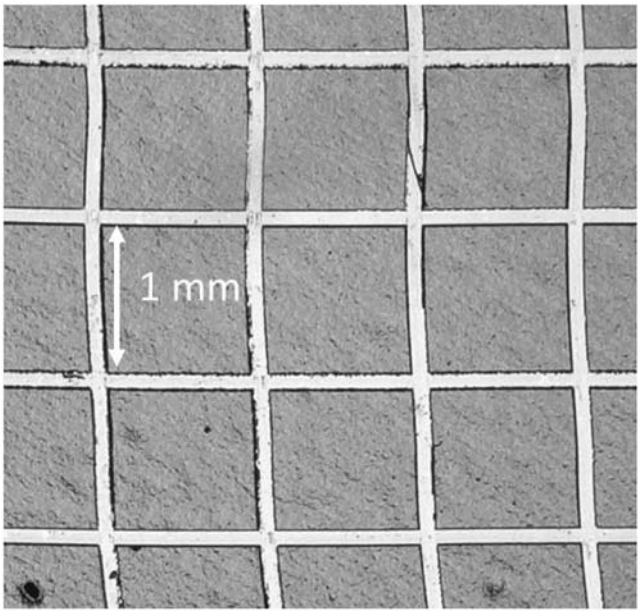


**FIGURE 9** 5B cross hatch result for black edge coating material

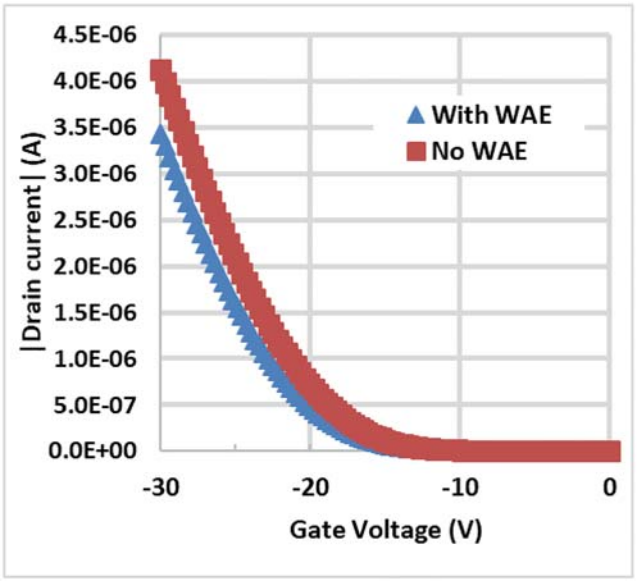


**FIGURE 10** LTPS TFT drain current as function of gate voltage. Blue triangles indicate TFT was driven using wrap-around electrodes

electrodes were deposited connecting the copper pads of the TFT to a backside interconnect. Figure 10 shows the TFT performance before and after the electrodes were deposited. The shift in threshold voltage was caused by slight oxidization of the copper pads attached to the TFTs because no annealing step was performed.

## 3 | IMPACT

To the best of our knowledge, this is the first paper reporting status and progress of wrap-around electrodes for tiled display applications. This approach offers an alternative to TGV technology to enable bezel-free tiles for microLED applications.


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*Note*: Sheet resistance was measured via Van der Pauw method, with current stepped between 0 and 10 mA in 0.1-mA steps, while other resistances were measured via kelvin 4-point probe method and best fit line of the IV curve for current stepped between 0 and 10 mA in 0.1-mA increments.


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